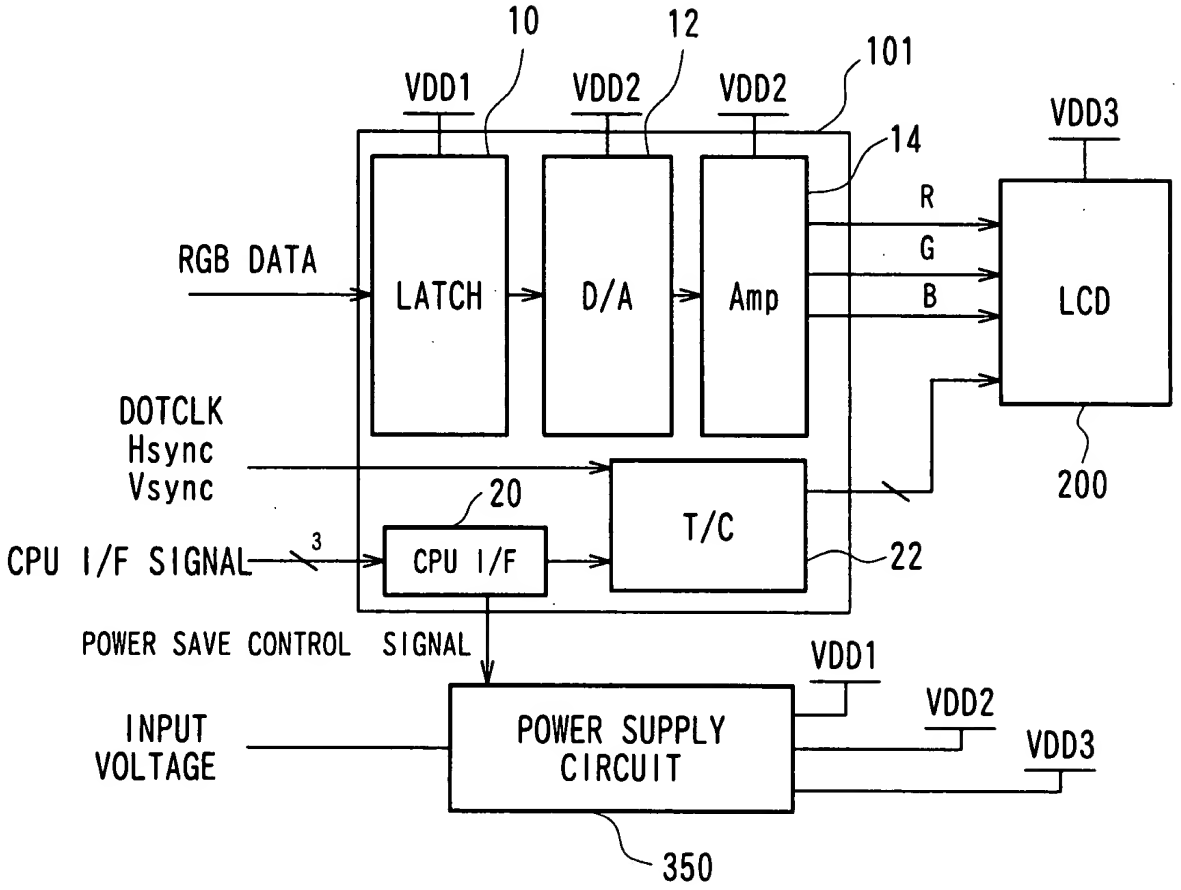

FIG. 1 RELATED ART

• SWITCHING REGULATOR

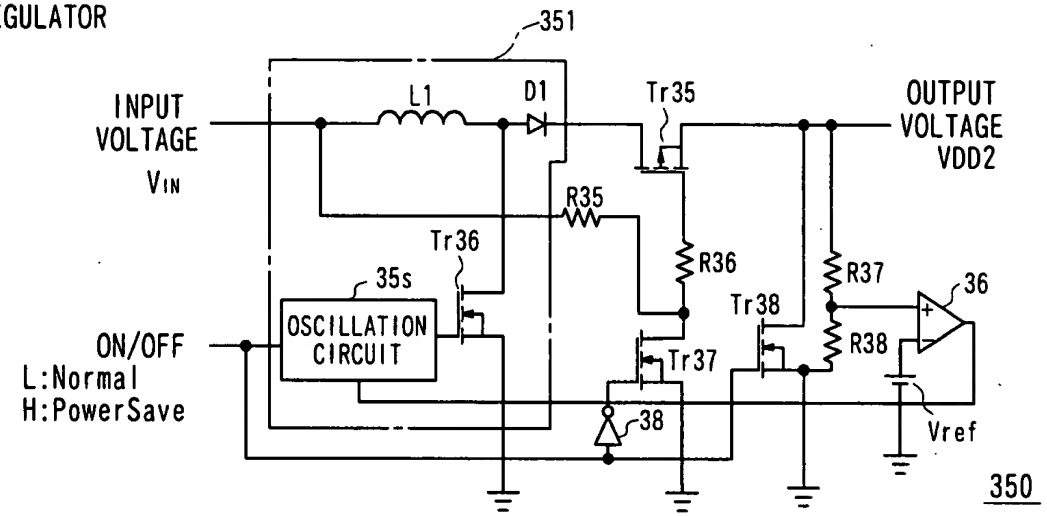

FIG. 2A RELATED ART

• CHARGE PUMP TYPE

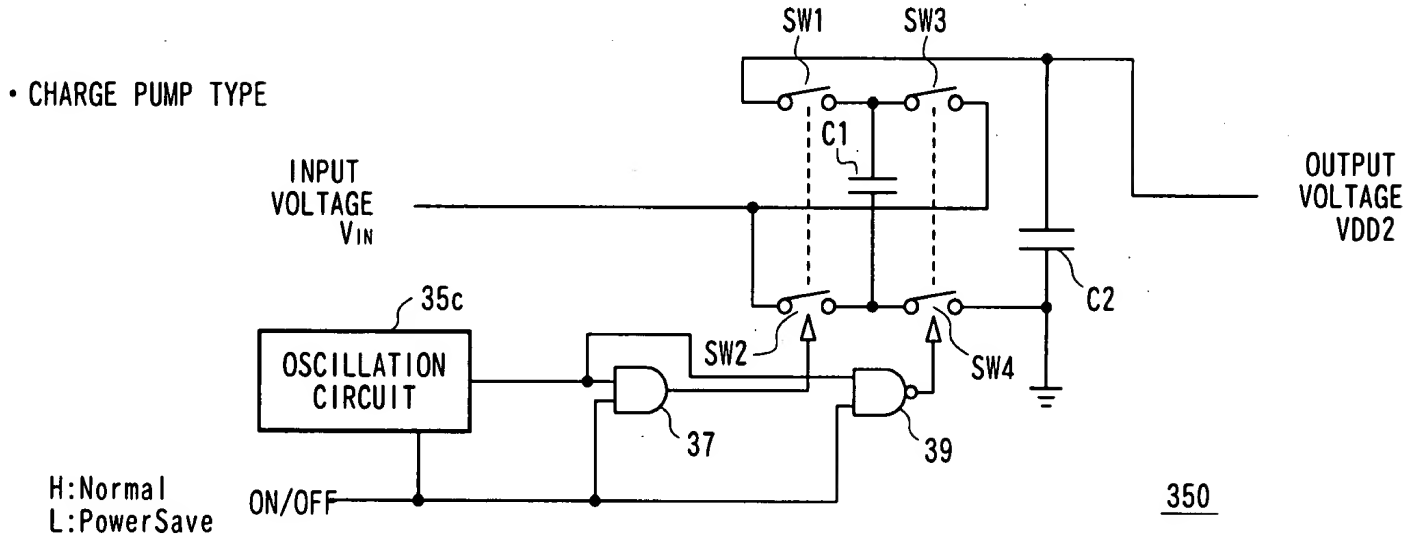

FIG. 2B RELATED ART

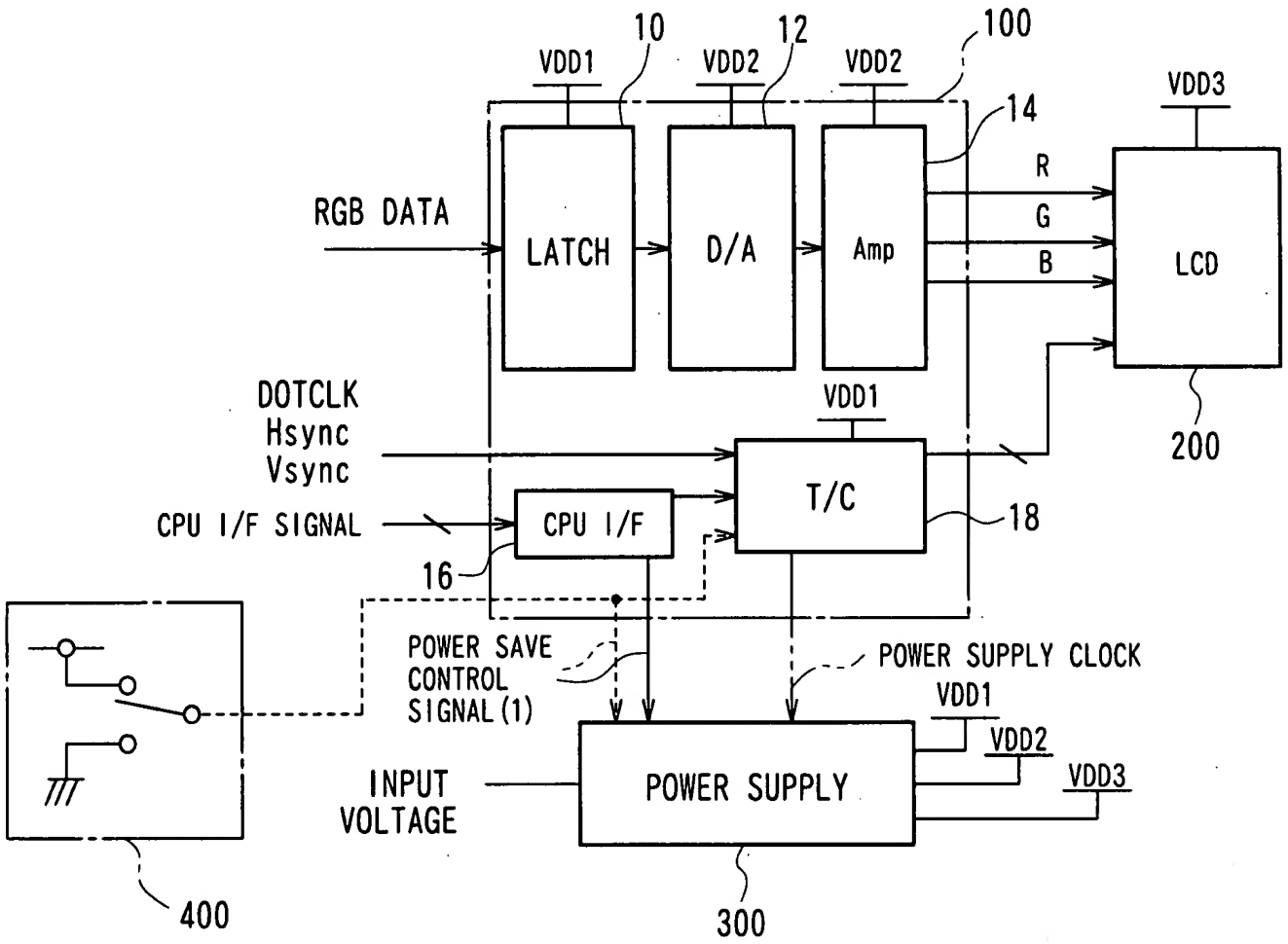
10
12
100
VDD1
VDD2
VDD2
VDD3
14
R
G
B
RGB DATA
LATCH
D/A
Amp
LCD
DOTCLK
Hsync
Vsync
VDD1
T/C
200
CPU I/F SIGNAL
CPU I/F
18
16
POWER SAVE
CONTROL
SIGNAL (1)
POWER SUPPLY CLOCK
VDD1
VDD2
VDD3
INPUT
VOLTAGE
POWER SUPPLY
400
300

FIG. 3

• SWITCHING REGULATOR

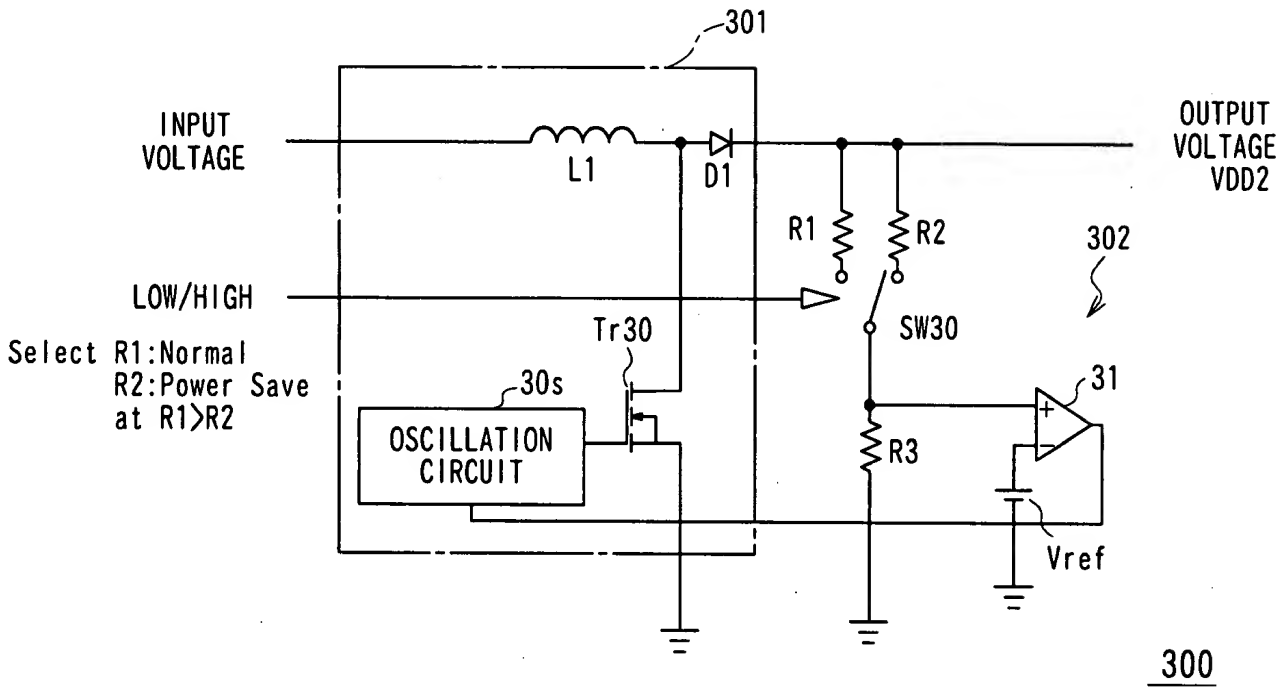

FIG. 4

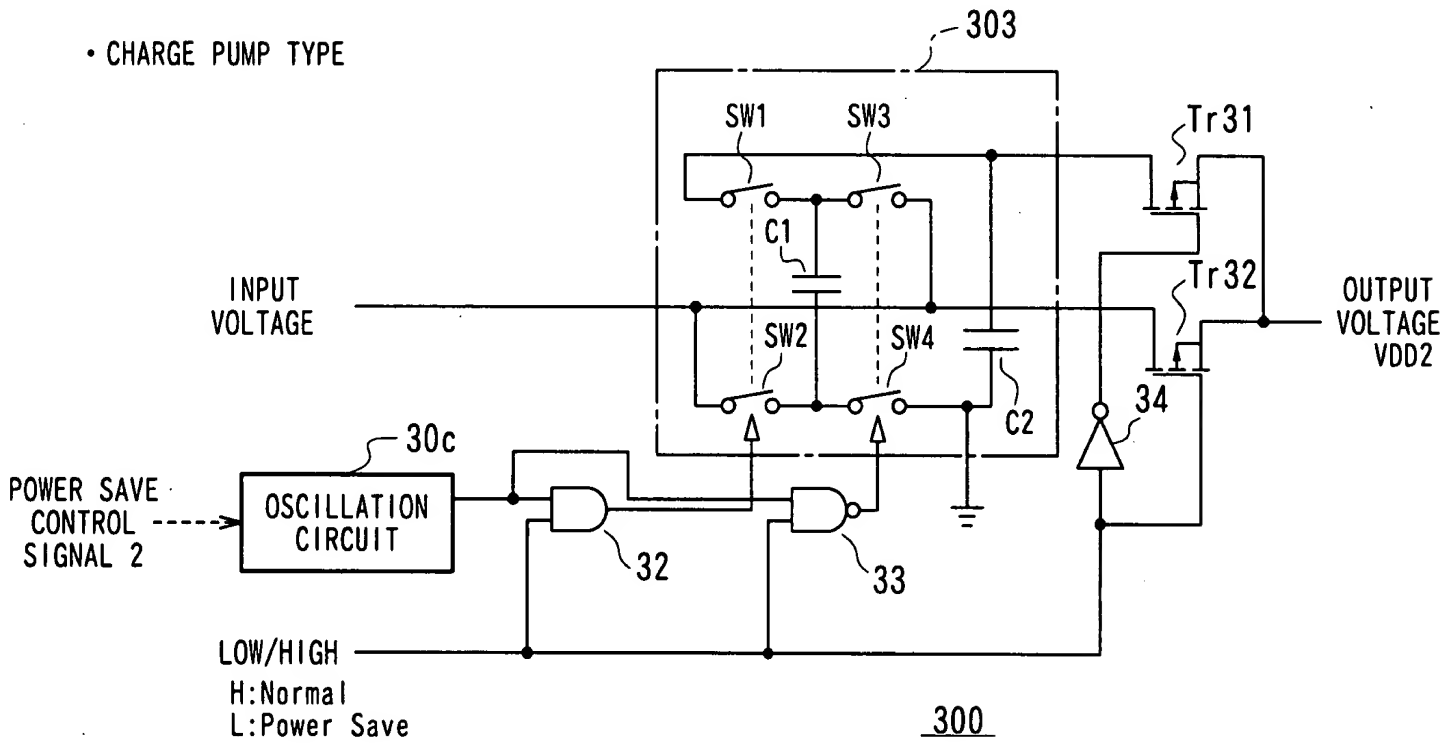

FIG. 5

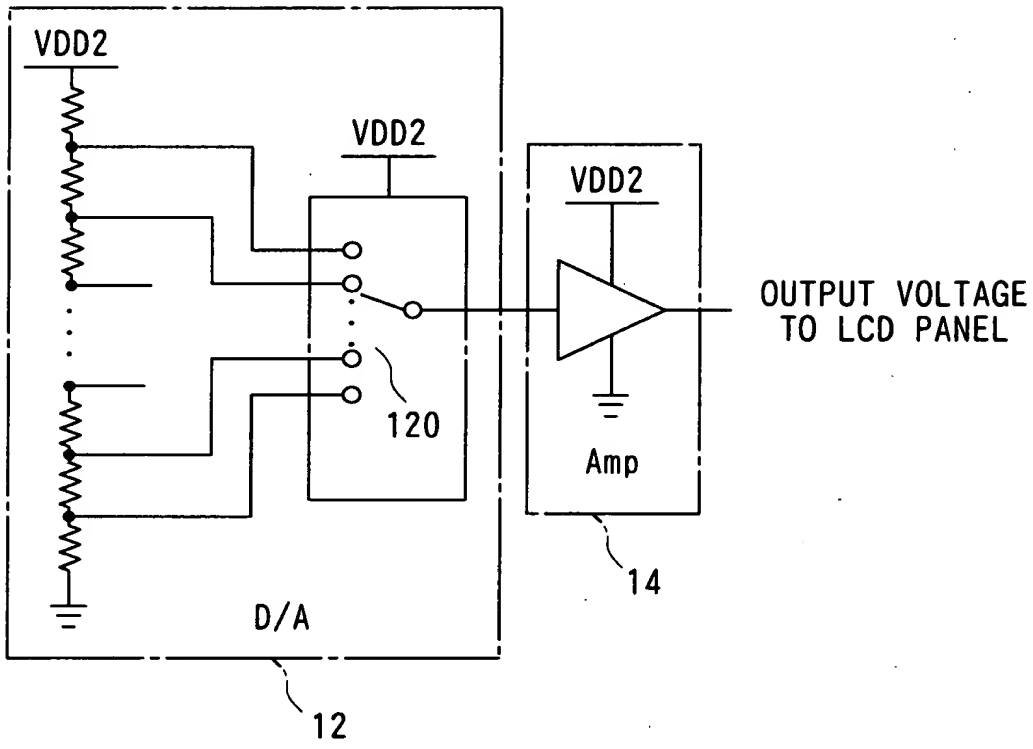

FIG. 6

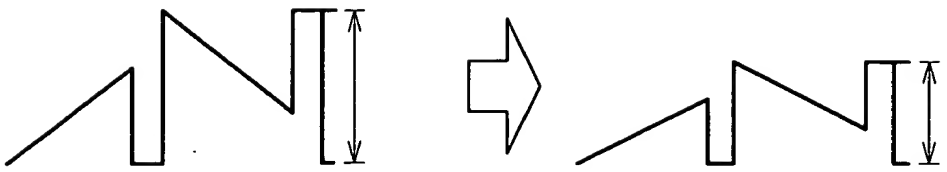

FIG. 7

• CHARGE PUMP TYPE

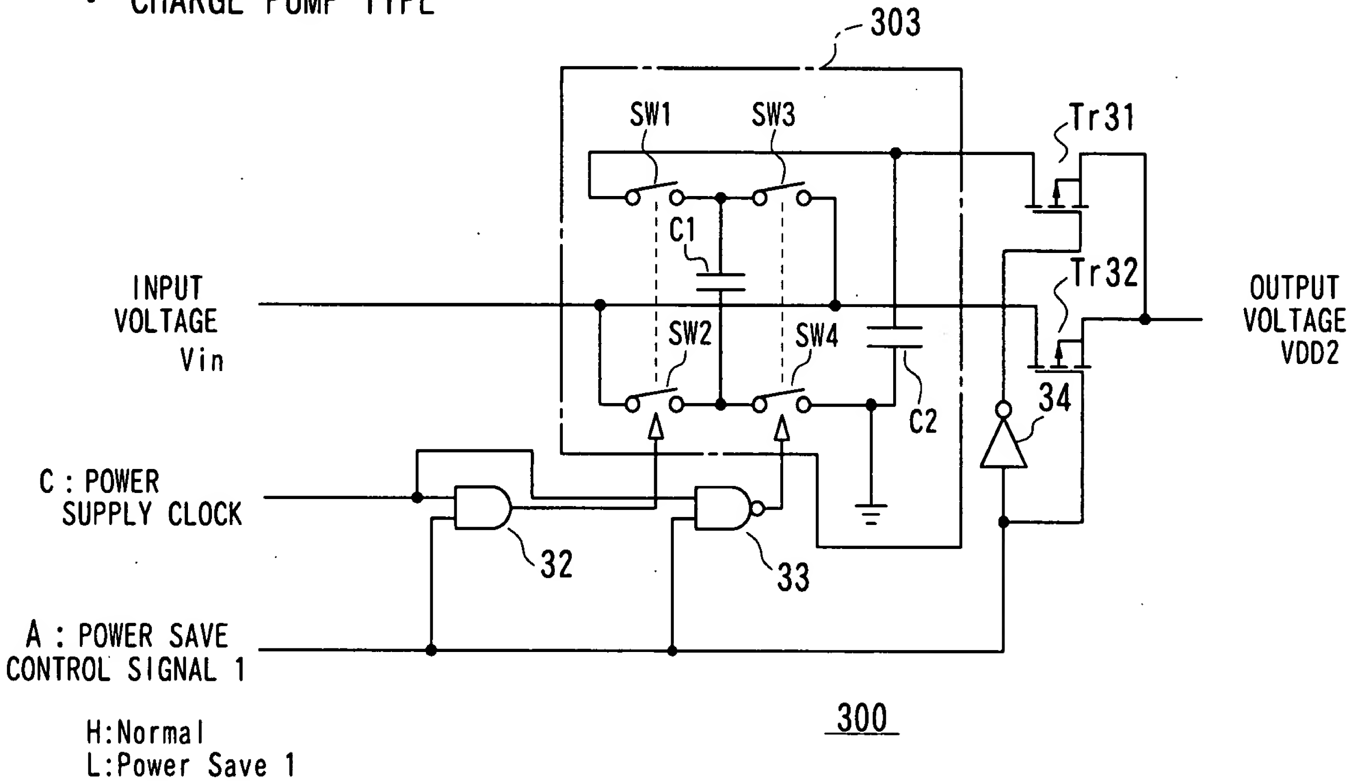

FIG. 8

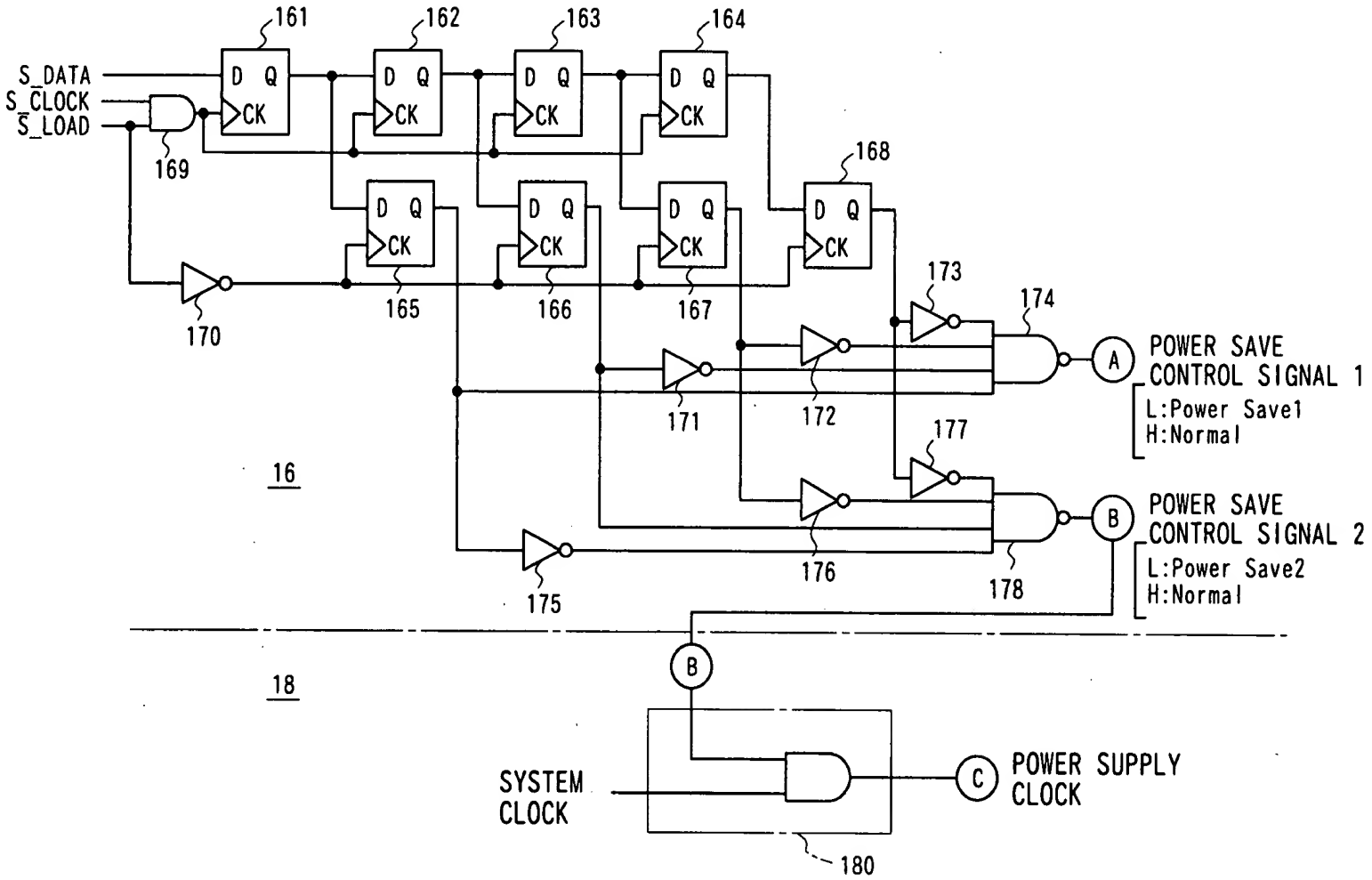
S_DATA
S_CLOCK
S_LOAD
161
162
163
164
168
169
170
165
166
167
173
174
171
172
177
176
178
175
16
18
A
B
C
POWER SAVE CONTROL SIGNAL 1
L:Power Save1
H:Normal
POWER SAVE CONTROL SIGNAL 2
L:Power Save2
H:Normal
SYSTEM CLOCK
POWER SUPPLY CLOCK
180

FIG. 9

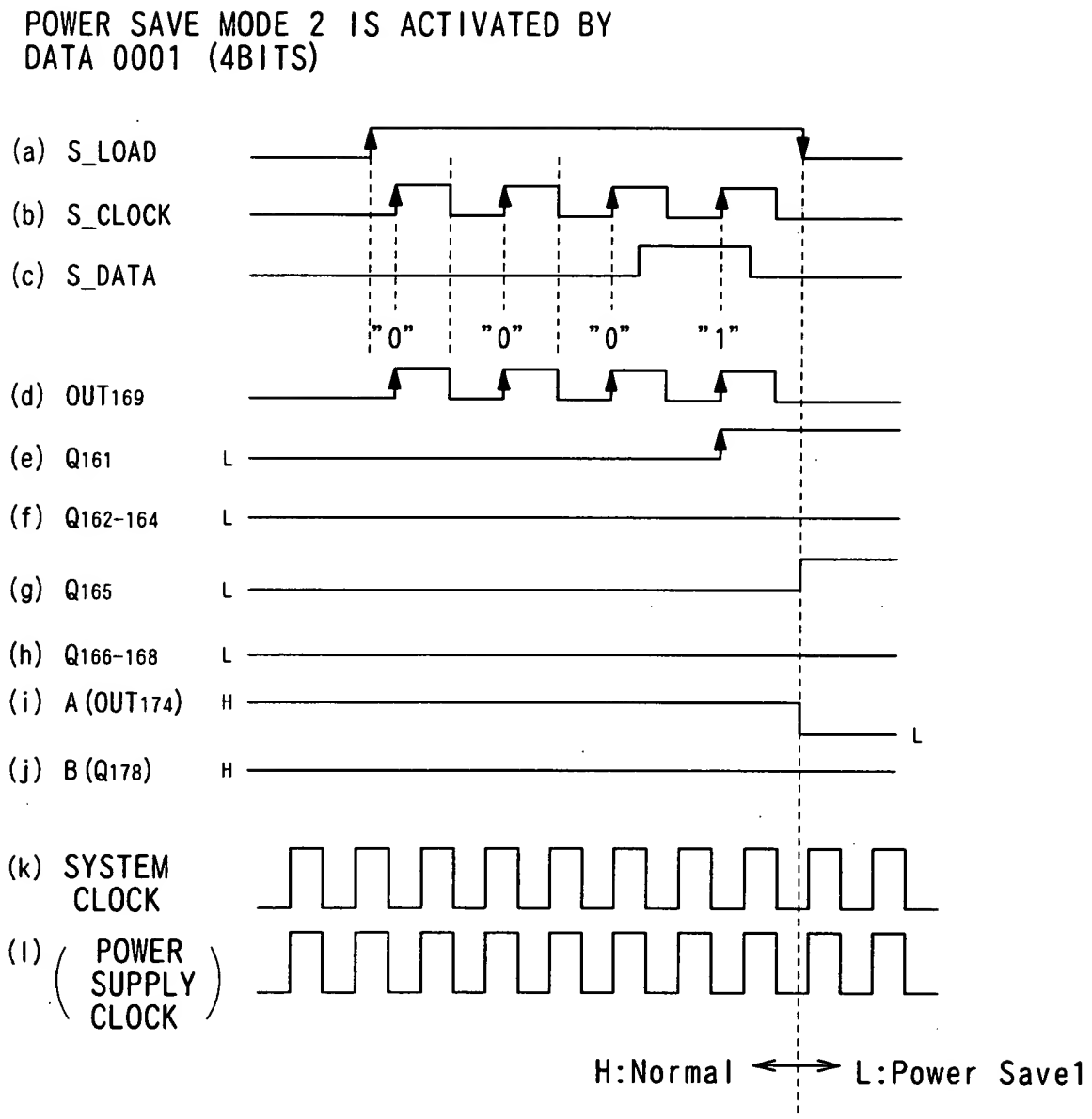
POWER SAVE MODE 2 IS ACTIVATED BY
DATA 0001 (4BITS)
(a) S_LOAD
(b) S_CLOCK
(c) S_DATA
"0"
"0"
"0"
"1"
(d) OUT169
(e) Q161
L
(f) Q162-164
L
(g) Q165
L
(h) Q166-168
L
(i) A (OUT174)
H
L
(j) B (Q178)
H
(k) SYSTEM CLOCK
(l) POWER SUPPLY CLOCK
H:Normal
L:Power Save1

FIG. 10

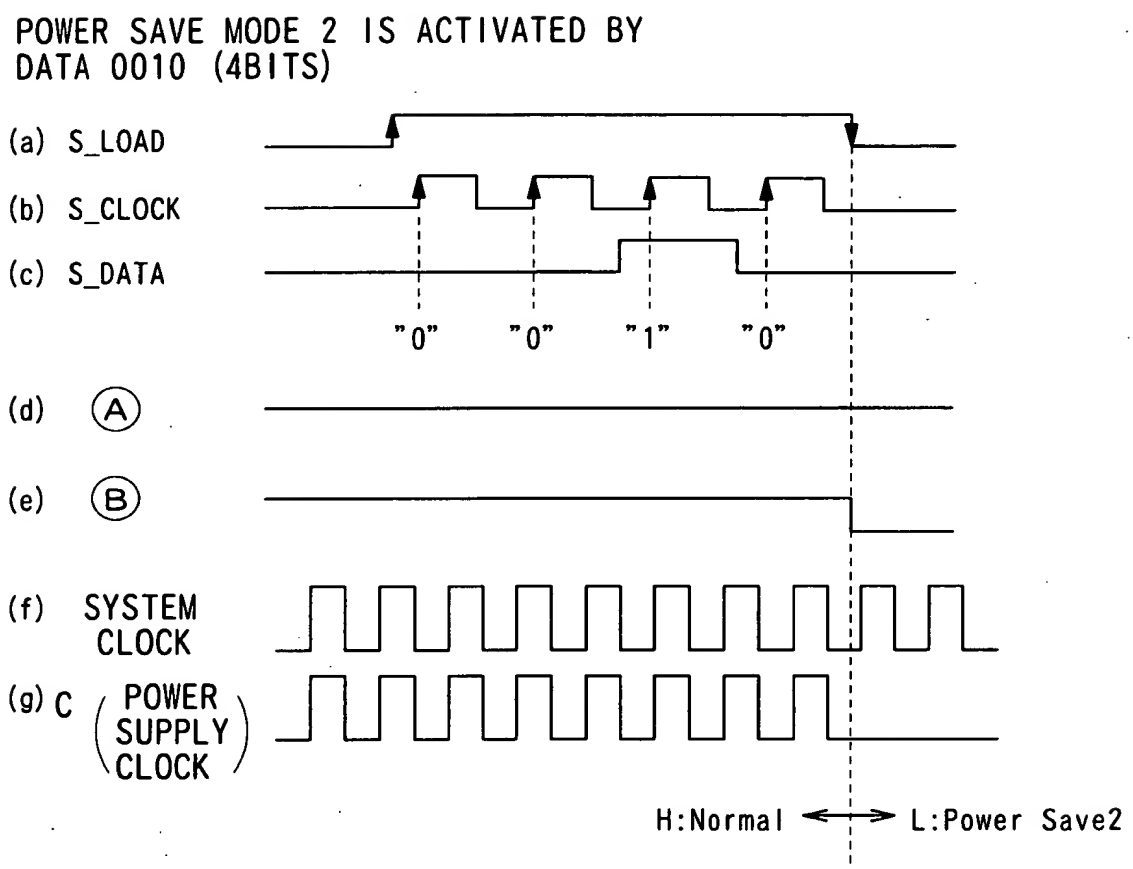
POWER SAVE MODE 2 IS ACTIVATED BY
DATA 0010 (4BITS)
(a) S_LOAD
(b) S_CLOCK
(c) S_DATA
"0"
"0"
"1"
"0"
(d) A
(e) B
(f) SYSTEM CLOCK
(g) C (POWER SUPPLY CLOCK)
H:Normal
L:Power Save2

FIG. 11